SOURCES OF NON-LINEARITY IN GaAs MESFET FREQUENCY MULTIPLIERS

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ABSTRACT

Transconductance and output conductance non-linearities of a single gate GaAs MESFET are used to define promising multiplier bias levels and harmonic loads. The model enables design of 25 mW 4-8 GHz doubler with 6 dB gain, 20 mW 4-12 GHz tripler with 3 dB gain and 2 mW 4-16 GHz quadrupler with 2 dB gain.

INTRODUCTION

Although the use of single-gate and dual-gate GaAs MESFET doublers is now well established [1-3] and analytical models have been presented [4,5] little attempt seems to have been made to explore, in a systematic fashion, optimal bias points and harmonic loads.
In this paper the major sources of non-linearity in a single gate GaAs MESFET are investigated both analytically and experimentally in order to determine optimum dc biasing points and harmonic load impedances. By these means, a GaAs MESFET (1 μm x 600 μm) + 4 GHz multiplier has been realized which gives the following excellent results : doubler (8 GHz), 6 dB gain with 25mW output power; tripler (12 GHz), 3 dB gain with 20 mW output power; quadrupler (16 GHz), 2 dB gain with 2 mW output power.

NON-LINEAR ANALYSIS

It has quickly become established that the main sources of non-linearity in a single gate GaAs MESFET are the transconductance, gm, and the output conductance, gd. Pumping the gate inpute to a common-source MESFET will yield, under appropriate bias conditions, harmonic products which can be enhanced or diminished by appropriate terminations. It was decided, in this work, to establish : (a) the dc bias conditions most conducive to harmonic generation, and (b) the harmonic terminations necessary to enhance successively production of 2nd, 3nd and 4 th harmonics.

A non-linear equivalent circuit model for the MESFET, figure 1, was selected and initial element values for the linear operating region were obtained in the usual manner. Next all element values, excepting gm and gd, were fixed. A campaign of S- parameter measure- between 500 MHz and 1 GHz was executed for a succession of static gate-source, Vgs, and drain-source, Vds, bias levels. Finally values of gm and gd that would permit the equivalent circuit to fit with S-parameter data at each bias level were calculated following reference [6]. From the results, figure 2, it is possible to select bias conditions and a fundamental load-line which favours harmonic generation due to gm (zone I), gd (zone II), or both (zone III for example).

A quasi-static approach is now applied, whereby gm (Vgs, Vds) and gd (Vgs, Vds) are transformed into large signal dynamic functions Gm (vg), Gd (vg) where vg (t) is a large-signal dynamic voltage applied to the gate. The transformation of gm and gd into Gm and Gd is effected by : a) selecting a load line to link unambiguously input voltage vg (t) and output voltage vd (t), and, b) the discretization of vg (t) into incremental steps, Δvg = vg (t+ Δ t)-vg (t). This permits the curves of figure 2 to be consulted either for a graphical analysis or a numerical analysis. Finally a Fourier analysis is used to transform Gm (t) and Gd (t) into the frequency domain.

Initial analysis indicated that optimum dc bias points for rich harmonic generation are near pinch-off, (zone I), or near Vgs = 0, (zone II). From figures 2 (a) and 2 (c), zone I requires a short-circuit load-line on transistor output and Vds = 4V. Zone II, figures 2 (b) and 2 (d), requires on the other hand an open-circuit load line and Vds = 2V.

EXPERIMENTAL RESULTS

Low Frequency Measurements

Experimental measurements with a fundamental frequency of 100 MHz were carried out in order to confirm the results of the theoretical analysis at frequencies under which harmonic terminations could easily be verified. Drain voltage waveforms under different bias and load conditions could equally be observed.

Zone I. Biasing the transistor near pinch-off and adjusting the output circuit for maximum second harmonic output power, resulted in an output impedance at the fundamental and third harmonic equal to a short circuit. Thus, non-linear transconductance is the predominant harmonic generator.

Zone II. When gate bias is changed to zero volts, optimum doubler operation is obtained with an output fundamental frequency open circuit load. In this case, the output conductance is the important non-linearity. It should be noted that when the dynamic input voltage is higher than 0.6 volts, gate current starts up with consequent voltage clipping. This unwanted phenomenon can be minimized by placing a high series resistance in the gate bias circuit, which self-biases the device (clamping effect). The drain voltage waveform, as observed by means of a sampling oscilloscope, is close to a half wave rectified sinusoid - a waveform rich in even harmonics.

Zone III. Vgs is maintained at zero volts, but terminal loads are changed : an open circuit for the fundamental, a short circuit for second harmonic. In this case Gm (t) as well as Gd (t) contribute to harmonic generation yielding the symmetrically distorted drain voltage waveform of figure 3, a characteristic of odd harmonic content.

Microwave Results : (4-8) GHz, (4-12) GHz and (4-16)GHz.

Zone I operation is akin to class - B operation : gain and power added efficiency increase rapidly with drive level reaching a maximum of 5 dB gain, and power added efficiency (ηadd) = 8% for an output power of 14 dBm. Above this level gain falls off, although ηadd and output power both continue increasing.

Zone II and III were favoured for harmonic generation, principally because input matching was easier to accomplish and efficient harmonic generation was obtained

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over a wide range of signal drive (10 dB). Thus a doubler gain of 6 dB was obtained for 14 dBm output power and η add = 4% for the circuit shown in figure 4.

For the quadrupler, the output circuit was more complex. Two $\lambda/8$ open circuit stubs at the fundamental frequency of 4 GHz followed by a high pass filter were used. A constant multiplier gain of 2 dB was measured for a 3 dB input power variation. Maximum non-saturated output power equalled 2 mW.

For tripler operation, the harmonic loads confirmed by low frequency measurements were applied as shown in figure 5. Lenghts 1. and 1 were selected to give appropriate reactive loads at the fundamental and second harmonic frequencies, while the band-pass filter was designed to let pass the 12 GHz third harmonic. Tripler gain of 3.0 dB and maximum Pout of 13 dB were obtained with add = 3%.

CONCLUSION

In this paper an analysis procedure has been developed for single-gate GaAs MESFET multipliers. The approach uses the non-linear variations of the transconductance, gm, and output conductance, gd, of the transistor, obtained by small-signal S-Parameter measurements over a wide range of bias points, to simulate multiplier behaviour. Thus d-c operating zones and harmonic and fundamental frequency loads are predicted and confirmed by v.h.f. and microwave results. The method has successfully permitted design of 4 GHz,/8 GHz, 4 GHz,/12 GHz, and 4 GHz/16 GHz multipliers as experimental results prove.

It should be noted that in this analysis, Cgd, drain-to-gate feedback capacitance has been neglected. This omission is being corrected in order to enable the model to be extended to higher frequencies.

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REFERENCES

1. Pan, J.J., IEEE MTT-S, Int. Microwave Symp. Dig., June 1978, pp. 306-308.
2. Gupta, M.S., Laton, R.W., and T.T. Lee, IEEE Trans. Microwave Theory Tech., MTT-29, March 1981, pp. 261-263.
3. Stancliff, R.B. and D.D. Poulin, IEEE MTT-S, Int. Microwave Symp. Dig., 1979, pp. 185-187.
4. Gopinath, A., and J.B. Rankin, IEEE Trans. Microwave Theory Tech., MTT-30, June 1982, pp. 869-875.
5. Rauscher, C., IEEEMMTT-S, Int. Microwave Symp. Dig., June 1982, pp. 280-282.
6. Perichon, R. A. and E. Camargo, to be published.
7. Rauscher, C. and H. A. Willing, IEEE Trans. Microwave Theory Tech., MTT- 27, October 1979, pp 834-840.

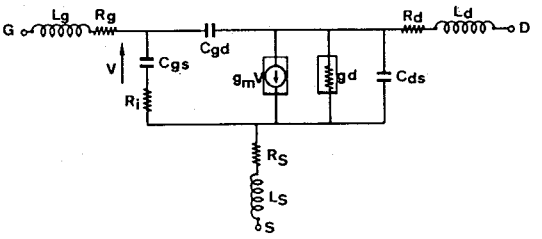

FIG 1:CIRCUIT MODEL OF A GaAs MESFET

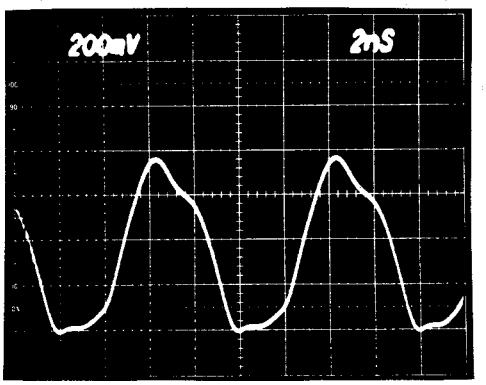

FIG 3 : SAMPLING OSCILLOSCOPE PHOTOGRAPH OF OUTPUT DRAIN VOLTAGE

Input voltage is equal to 0.7 volts peak at a fundamental frequency of 100 MHz. Vertical scale = 10 X.

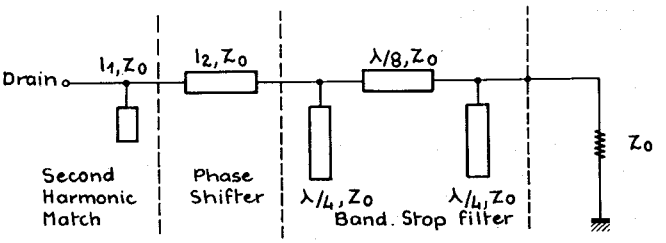

FIG 4 : HARMONIC LOAD FOR A DOUBLER CIRCUIT

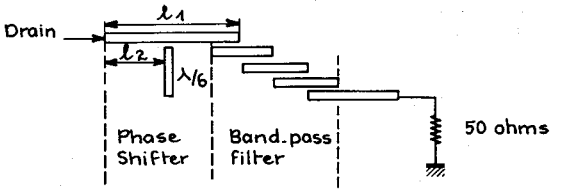

FIG 5 : HARMONIC LOAD FOR A TRIPLER CIRCUIT

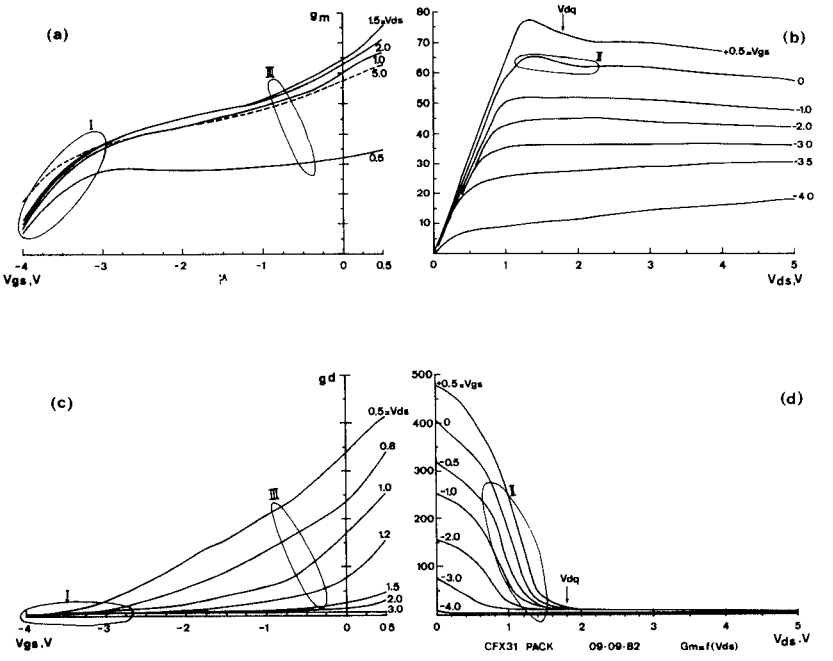

FIG 2 : NON-LINEAR ELEMENTS FUNCTION OF Vgs and Vds.